Amendments to the Claims

This listing of claims will replace all prior listings of claims in the application.

Listing of Claims

1. (Currently Amended) A memory device comprising an array of bits or binary units, the bits being defined by a plurality of first conductors and either a second conductor or a plurality of second conductors overlying and separated from the first conductors, each bit including a cross-over point between one of the first conductors and the second conductor, or one of the second conductors, and wherein ~~a selection of the bits also include~~the status of each bit or binary unit is determined by the presence or absence of a signal bridge connecting the first and second conductors at ~~each of~~ the respective ~~selected pixels~~cross-over point.

2. (Currently Amended) A memory device according to claim 1 wherein the plurality of first conductors are substantially parallel to each other and substantially orthogonal to the second conductor or conductors, and the plurality of second conductors are substantially parallel to each other.

3. (Previously Presented) A device according to claim 1 wherein the signal bridge is a capacitor.

4. (Previously Presented) A device according to claim 1 wherein the signal bridge is a contact bridge.

5. (Currently Amended) A memory device according to claim 1 comprising an insulating layer between the first and second conductors, the insulating layer including a signal via at each of the ~~selected bits~~cross-over points through which

said ~~contact bridge connects~~signal bridges connect the respective first and second conductors ~~at each said selected bit~~.

6. (Currently Amended) A memory device according to claim 1 comprising a bit map or bit pattern layer having a pattern of ~~overlying the array of bits and~~ conductive elements forming contact bridges on a surface overlying the array of cross-over points for connecting ~~a selected portion of the first and second conductors at a selected portion of the cross-over points between the conductors~~ each of those cross-over points through which a said contact bridge connects the respective first and second conductors at the respective cross-over point.

7. (Currently Amended) A memory device according to claim 6 wherein there are switch means on a surface of the array of bits or cross-over points and associated with each bit or cross-over point, each switch means including a first contact portion of one of the first conductors and a second contact portion of the second conductor or one of the second conductors wherein the first and second contact portions of each bit or cross-over point are separated from one another, and the contact portions of predetermined selection of the bits or cross-over points are connected by the contact bridges of the overlying bitmap or bit pattern layer to connect the first and second conductors at each pre-determined selected cross-over point.

8. (Previously Presented) A memory device according to claim 5 wherein the insulating layer is a thin sheet of a plastics material such as a polyimide, polyester, polystyrene or polyethylene.

9. (Currently Amended) An identifying or transaction card, for example, a credit card, debit card, identity card,

driving ~~licence~~license, passport, or social security card including a memory device according to claim 1 programmed with identification data or information characteristic or personal to the ~~authorised~~authorized user or users of the card.

10. (Original) A card according to claim 9 further comprising a fingerprint sensor.

11. (Original) A card according to claim 10 comprising a matrix of cells, each cell being defined by a cross-over point between one of a plurality of parallel first conductors and one of a plurality of parallel second conductors overlying and separated from the first conductors, wherein a first portion of the matrix is the memory device and a second portion of the matrix is a fingerprint sensor, wherein the cells of the first memory device portion are the bits of the memory device, and the cells of the second fingerprint sensor portions are the sensing cells of a fingerprint sensor, the card also including a resiliently deformable membrane overlying the second fingerprint sensor portion of the matrix, the membrane having conductive portions on its underside to connect the first and second conductors of one or more sensing cells in response to the presence or absence of a fingerprint ridge pressing down on the deformable membrane.

12. (Currently Amended) A card according to claim 11 wherein the second memory device portion includes a first memory section for storing a selected fingerprint pattern, and a second memory section for storing information about a selected ~~authorised~~authorized user or selected ~~authorised~~authorized users of the card.

13. (Original) A card according to claim 12 wherein the first memory section is adjacent and contiguous to the fingerprint sensor portion, and the second memory section is

adjacent and contiguous to the first memory section and the fingerprint sensor portion.

14. (Previously Presented) A card according to claim 11 wherein the card includes a set of drive electrodes connected to the first (or second) conductors for supplying signals thereto and a set of sensing electrodes connected to the second (or first) conductors for monitoring the output therefrom.

15. (Original) A card according to claim 14 wherein a single set of drive electrodes and a single set of sensing electrodes may be used to address or interrogate both the memory device and the fingerprint sensor.

16. (Currently Amended) A method of making a memory device comprising an array of bits, the method comprising the steps of:

providing an insulating support;

~~to~~ forming a plurality of first conductive portions on a first surface of the support;

~~to~~ forming a second conductive portion or a plurality of second conductive portions on a second surface of the support, ~~and~~ separated from and crossing the first conductive portions at cross-over locations; and

corresponding to the locations of the signal vias providing signal vias extending through the insulating support at selected cross-over locations;

wherein to establish an electrical coupling is established between respective first and second conductive portions at the selected cross-over locations through the signal vias;

wherein the status of each bit is determined by the presence or absence of a signal via at the respective cross-over location.

17. (Original) A method according to claim 16 wherein the signal vias are provided by drilling holes extending through or partly through the insulating support and the walls of the holes are coated with a conductive material.